Claims of the invention

1. A signal processing method comprising:

a first step for decoding an encoded information data series and forming a decoded data series;

a second step for detecting decoded data in said decoded data series that cannot exist in said information data; and

a third step for decoding said information data series again using information relating to said detected decoded data, and forming a decoded data series.

2. A signal processing method as described in claim 1 wherein:

a readback signal sequence from a recorded information medium is used as said encoded information data series;

maximum-likelihood sequence decoding is used for said decoding; and

said third step is performed repeatedly on said readback signal sequence using said maximum-likelihood sequence decoding.

3. A signal processing method as described in claim 1 wherein said information relating to said detected decoded data is at least one of the following: (1) a position of said detected decoded data within said decoded data series; and (2) the contents of said detected decoded data.

4. A signal processing method as described in claim 1 wherein said information relating to said detected decoded data is at least one of the following: (1) a position at which decoded data other than said detected decoded data is present within said decoded data series; and (2) the contents of said decoded data other than said detected decoded data.

5. A signal processing method as described in claim 1 wherein:

said second step includes a step for correcting said decoded data that cannot exist in said information data: and

said third step is performed if applying correction is impossible to all said decoded data that cannot exist in said information data from said second step.

6. A signal processing method as described in claim 5 wherein:

said first step forms a decoded data series divided into a plurality of code series: and

said second step performs detection and correction of said decoded data that cannot

exist in said information data independently for each of said plurality of code series.

7. A signal processing method as described in claim 5 wherein a code sequence of said decoded data series is changed prior to said second step.

8. A signal processing device comprising:

a decoding circuit decoding an information data series and forming a decoded data series;

an error data detection circuit detecting decoding error data in said decoded data series and sending out error information relating to said decoding error data; and

a feedback signal path sending said error information from said error data detection circuit to said decoding circuit;

wherein said decoding circuit uses said error information to process a section of said information data series that has already been processed.

9. A signal processing device as described in claim 8 wherein:

said error data detection circuit includes a function for correcting decoding error data; and

said decoding circuit uses said error information to process a section of said information data series that has already been processed only when said error data detection circuit is unable to completely correct decoding error data.

10. A signal processing device as described in claim 8 wherein said error data detection circuit includes a divider circuit dividing a decoded data series output from said decoding circuit into a plurality of code series and a plurality of error data detection element circuits processing each of said plurality of code series.

11. A signal processing device as described in claim 9 wherein said decoding circuit is a maximum-likelihood sequence decoding circuit using maximum-likelihood sequence decoding that determines a single data series that appears most reliable out of a plurality of candidate decoded data series.

12. A signal processing device as described in claim 11 wherein said error information is formed from information (position and contents) relating to data determined by said error data detecting means not to contain decoding error data (correct data) in said readback data series. or information (position and corrected contents) relating to data for which decoding error data was

found and corrected by said error data detecting means.

13. A signal processing device as described in claim 12 wherein, when said error information is used by said decoding circuit and a section of said information data series that has already been processed is processed again, said error information is referred to in order to eliminate data not matching data indicated by said error information from said candidate decoded data series.

14. A signal processing device as described in claim 12 wherein, when said error information is used by said decoding circuit and a section of said information data series that has already been processed is processed again, said error information is referred to in order to use data matching data indicated by said error information as data for said candidate decoded data series.

15. In an information recording/readback circuit including:

a maximum-likelihood sequence decoding circuit receiving a readback signal sequence from a recorded information medium as input, performing conversion into a readback data code series corresponding to said recorded information, and outputting results of said conversion: and

an error data detection/correction circuit receiving said converted readback data code series as input, checking for presence of decoding error data codes (readback data codes not corresponding to said recorded information) in said readback data code series, and correcting and outputting said detected decoding error data code as correct data code;

an information readback circuit comprising:

a memory circuit storing said readback signal sequence;

wherein:

partial code information (code position and code values) of said readback data code sequence detected by said error data detection/correction circuit is fed back to said maximum-likelihood sequence decoding circuit as input: and

said maximum-likelihood sequence decoding circuit uses said partial code information and repeatedly converts said readback signal sequence stored in said storage circuit into said readback data code sequence.

16. An information readback circuit as described in claim 15 wherein said partial code information fed back as input to said maximum-likelihood sequence decoding circuit is formed from information (code position and code value) relating to data determined by said error data detection/correction circuit not to contain decoding error data (correct data code) in said readback data series, or information (code position and corrected code values) relating to data for which decoding error data was found and corrected by said error data detection/correction circuit.

17. An information readback circuit as described in claim 15 wherein said repeated conversion to said readback data code sequence by said maximum-likelihood sequence decoding circuit is performed when said error data detection/correction circuit finds decoding error data codes in said readback data code sequence and correction of all said detected decoding error data codes is not possible.

18. An information readback circuit as described in claim 15 wherein:
said readback data code series output from said maximum-likelihood sequence decoding circuit is divided into a plurality of code series; and
said data detection/correction circuit detects error data codes and performs corrections on each of said plurality of code series independently.

19. An information readback circuit as described in claim 15 wherein:

said readback data code series output from said maximum-likelihood sequence decoding circuit is divided into a plurality of code series and sent separately into said plurality of error data detector/corrector circuits for detection and correction of error data code. the results thereof being output from said error data detector/corrector circuits;

when one of said plurality of error data detection/correction circuits outputs an indication that decoding error data code in an incoming code series cannot be corrected. a selector circuit selectively outputs part or all of code information from either an input signal for a data detection/correction circuit other than said error data detection/correction circuit or an output code series; and

output from said selector circuit is sent to said maximum-likelihood circuit.

20. An information readback circuit as described in claim 15 wherein:

when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) a code series not matching said partial code information is eliminated from maximum-likelihood candidate code sequences. degrees of likelihood for said maximum-likelihood candidate code sequences are compared. and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected; and

(2) only code sequences matching said partial code information are set up as maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared. and a readback data code sequence (maximum-

likelihood sequence) corresponding to said readback signal sequence is selected.

21. An information readback circuit as described in claim 15 wherein:

when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) code sequences in which a code position (time) indicated in said code information being used does not contain a corresponding code value are eliminated from maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected; and

(2) only code sequences in which a code position (time) indicated in said code information being used contains a corresponding code value are set up as maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected.

22. An information readback circuit as described in claim 15 wherein:

said maximum-likelihood decoding circuit selects a readback data code sequence (maximum-likelihood code sequence) using a Viterbi algorithm;
when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) code sequences in which a code position (time) indicated in said code information being used does not contain a corresponding code value are eliminated from maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected; and

(2) only code sequences in which a code position (time) indicated in said code information being used contains a corresponding code value are set up as maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected.

23. An information readback circuit as described in claim 15 wherein:

said maximum-likelihood decoding circuit selects/estimates a readback data code

sequence (maximum-likelihood code sequence) using a predetermined code state transition diagram;

when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) for a transition position (time) on said code state transition diagram corresponding to a code position (time) indicated by said code information being used, said readback data code sequence (maximum-likelihood code sequence) is selected/estimated using a code state transition diagram from which state transitions or code states not indicated by said code value are eliminated;

(2) for a transition position (time) on said code state transition diagram corresponding to a code position (time) indicated by said code information being used, said readback data code sequence (maximum-likelihood code sequence) is selected/estimated using a code state transition diagram in which only state transitions or code states indicated by said code value are left.

24. An information readback circuit as described in claim 15 further comprising a code interleaving circuit changing a code sequence of said readback data code series before said error data detection/correction circuit detects decode error data and performs correction.

25. An information readback circuit as described in claim 24 wherein:

said code interleaving circuit changing a code sequence of said readback data code series changes the sequence of said readback data code series using blocks of consecutive code having a predetermined length as units; and

said code interleaving circuit changing the sequence in said readback data code series so that consecutive code blocks are separated.

26. An information readback circuit as described in claim 25 wherein said code length of said code block is no more than a code length of a code block serving as a processing unit for detection and correction of decoded error data codes by said error data detecting/correcting means.

27. An information readback circuit as described in claim 14 wherein said readback signal sequence from said recorded information medium is sent to said maximum-likelihood sequence decoding circuit via a predetermined partial response signal transfer system.

28. An information readback circuit as described in claim 15 wherein said readback signal sequence from said recorded information medium is not resent as input during repeated conversion to readback data code sequence performed by said maximum-likelihood sequence

decoding circuit.

29. A data processing method comprising the following steps:

(1) a first step for receiving an encoded information data series as input;

(2) a second step for decoding said encoded information data series and generating a first decoded data code series by selecting a single candidate decoded data code series out of a first candidate decoded data code series group;

(3) a third step for detecting a position and content of an erroneous decoded data code in said first decoded data code series not matching said information data code;

(4) a fourth step correcting said erroneous data code and generating a corrected data code;

(5) a fifth step decoding said encoded information data code series again and generating a second decoded data code series by selecting a single decoded data code series from a second candidate decoded data code series group;

(6) said second candidate decoded data code series group being formed from candidate decoded data code series from said first candidate decoded data code series group fulfilling at least one of the following conditions:

1. a candidate decoded data code series not containing erroneous decoded data codes that were detected at said third step and that could not be corrected at said fourth step;

2. a candidate decoded data code series containing data codes determined at said third step to not be an erroneous decoded data code and corrected data codes corrected at said fourth step.

30. A data processing method as described in claim 29 wherein a code interleaving step for changing a code sequence of said first decoded data code series precedes said third step.

31. A data processing method as described in claim 29 wherein said encoded information data series is received as input via a partial-response signal transfer system.

32. A data processing method as described in claim 29 wherein in said fifth step an encoded information data code series stored in memory is decoded again to generate a second decoded data code series.

33. An integrated circuit device (LSI) comprising:

a decoding circuit decoding an information data series and generating a decoded data series:

an error data detecting circuit detecting decode error data in said decode data series and outputting error information regarding said decode error data; and

a feedback signal path sending said error information from said error data detecting circuit as input to said decoding circuit;

wherein said decoding circuit uses said error information and re-processes an information data series that has been processed once at the same position.

34. An information recording device comprising:

an information readback circuit reading back an information data series from a recording medium; and

an integrated circuit device, said integrated circuit device including:

a decoding circuit decoding said information data series from said information readback circuit and generating a decoded data series;

an error data detecting circuit detecting decoding error data in said decoded data series and outputting error information relating to said decode error data;

and a feedback signal path sending said error information from said error data detecting circuit as input to said decoding circuit;

said decoding circuit using said error information to re-process an information data series that has been processed once at the same position.